INTEGRATED CIRCUIT CELLS

ABSTRACT OF THE DISCLOSURE

According to one embodiment of the invention, a method for designing an integrated circuit is provided. The method includes providing a first transistor in a first logic path. The first transistor has a first contact, a first gate length and a first contact to gate centerline spacing. The method also includes providing a second transistor in a second logic path. The second transistor has a second contact, a second gate length and a second contact to gate centerline spacing. The first contact to gate centerline spacing is substantially equal to the second contact to gate centerline spacing. The method also includes selecting a different gate length for the first gate length using a predetermined design criterion.